a first pad arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot;

a second pad arranged on a wiring level different from said first I/O slot and arranged apart from the peripheral portion of the chip as compared with the first pad;

a first wiring comprising one end positioned in said first pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

Cont'd C1

a second wiring comprising one end positioned in the second pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot; and

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot.

C2

10. (Twice Amended) The semiconductor integrated circuit device according to claim 1, further comprising a fourth wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, wherein the third wiring is isolated from the second wiring, and the fourth wiring is isolated from the first wiring.

C3

15. (New) The semiconductor integrated circuit device according to claim 1, wherein the I/O slot different from the first I/O slot is the second I/O slot.

16. (New) The semiconductor integrated circuit device according to claim 1, wherein the first and second pads are arranged on the same wiring level.

17. (New) The semiconductor integrated circuit device according to claim 1, wherein the first and second I/O slots are adjacent to each other.

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